

**AMENDMENTS TO THE CLAIMS**

1 – 8 (canceled)

9. (Currently amended) A flash memory device comprising:

- a plurality of n-wells comprising an n-type conductivity material formed in a p-type substrate;
- a plurality of p-wells comprising a p-type conductivity material, each p-well located within a different n-well;
- a plurality of flash memory array blocks, each comprising a plurality of flash memory cells arranged in rows that are coupled together by a first set of wordlines of a plurality of sets of wordlines, each flash memory array block located within a different p-well of the plurality of p-wells wherein a voltage differential of 5V is applied between the n-well and the p-well of an unselected flash memory array block during an erase operation; and
- a first row decoder coupled to the plurality of memory array blocks through the first set of wordlines, external address signals coupled to the first row decoder such that a wordline of the first set of wordlines is selected in response to the address signals.

10. (canceled)

11. (Original) The flash memory device of claim 9 wherein a voltage of 5V is applied to the n-well and a voltage of 5V is applied to the p-well of an unselected flash memory array block during a program operation.

12. (canceled)

13. (currently amended) A flash memory device comprising:

- a plurality of lower wells comprising a first conductivity material formed in a substrate comprising a second conductivity material;
- a plurality of isolation wells comprising the second conductivity material, each isolation well located within a different lower well;

a plurality of flash memory array blocks, each comprising a plurality of flash memory cells arranged in rows that are coupled together by a first set of wordlines of a plurality of sets of wordlines, each flash memory array block located within a different isolation well of the plurality of isolation wells wherein a voltage differential of 5V is applied between the lower well and the isolation well of an unselected flash memory array block during an erase operation; and  
a first row decoder coupled to the plurality of memory array blocks through the first set of wordlines, external address signals coupled to the first row decoder such that a wordline of the first set of wordlines is selected in response to the address signals.

14. (canceled)

15. (Previously Presented) The flash memory device of claim 13 wherein a voltage of 5V is applied to the lower well and a voltage of 5V is applied to the isolation well of an unselected flash memory array block during a program operation.

16. (Previously Presented) The flash memory device of claim 13 wherein the first conductivity material is an n-type conductivity material.

17. (Previously Presented) The flash memory device of claim 13 wherein the second conductivity material is a p-type conductivity material.

18. (currently amended) A method for programming a memory cell in a memory array block of a plurality of memory array blocks, each memory array block located within a first conductivity material that is located within a second conductivity material, the method comprising:  
generating an address signal of the memory cell;  
a row decoder selecting, in response to the address signal, a wordline signal that is coupled to the memory cell, the wordline signal additionally coupled to the plurality of memory array blocks;

coupling a first voltage that is greater than 0V to the first conductivity material of memory array blocks that are not selected by the wordline signal; and  
coupling a second voltage that is greater than 0V to the second conductivity material of memory array blocks that are not selected by the wordline signal. wherein a voltage differential of 5V is applied between the first conductivity material and the second conductivity material of an unselected memory array block.

19. (canceled)

20. (currently amended) A method for erasing a memory cell in a memory array block of a plurality of memory array blocks, each memory array block located within a first conductivity material that is located within a second conductivity material, the method comprising:

generating an address signal of the memory cell;

a row decoder selecting, in response to the address signal, a wordline signal that is coupled to the memory cell, the wordline signal additionally coupled to the plurality of memory array blocks; and

coupling a voltage that is substantially equal to -5V less than 0V to the second conductivity material of memory array blocks that are not selected by the wordline signal.

21. (canceled)

22. (currently amended) An electronic system comprising:

a processor that controls operation of the electronic system and generates address signals;  
and

a flash memory device coupled to the processor, the device comprising:

a plurality of lower wells comprising a first conductivity material formed in a substrate comprising a second conductivity material;

a plurality of isolation wells comprising the second conductivity material, each isolation well located within a different lower well;

- a plurality of flash memory array blocks, each comprising a plurality of flash memory cells arranged in rows that are coupled together by a first set of wordlines of a plurality of sets of wordlines, each flash memory array block located within a different isolation well of the plurality of isolation wells wherein a voltage differential of 5V is applied between the lower well and the isolation well of an unselected flash memory array block during an erase operation; and
- a first row decoder coupled to the plurality of memory array blocks through the first set of wordlines, external address signals coupled to the row decoder such that a wordline of the first set of wordlines is selected in response to the address signals.